REMARKS

This is in response to the Office Action dated November 24, 2006. Examiner's previous allowance of claims 1-3, 5, 6, 11-14, and 17-29 has been withdrawn. Claims 1-3, 5, 6, 10-14, and 17-29 (all the claims) have been rejected. In order to more succinctly set forth their invention, applicants have added claims 30-45. These claims have been drafted with a view to overcoming the rejections under 35USC112. Concurrently, claims 1-3, 5, 6, 10-14, and 17-29 (all the previously allowed claims) have been canceled. Examiner has also raised objections with respect to the drawings and specification.

Regarding the drawings, 5 Replacement Sheets are attached to a Letter to the Chief Draftsman enclosed herewith. In addition to Examiner's comments, Applicants noted that FIGs. 1-3 depict Prior Art and these Figures have been marked accordingly. Tx and Rx have been reversed to correct the clerical error noted by Examiner. Regarding "SERDES", this is a well known acronym for a serializer-deserializer and was placed on the Prior Art drawing with that understanding. However, in view of Examiner's objection, it has been deleted from the drawings. The remaining legend: "FREQUENCY COMPENSATION" adequately describes the Prior Art system that is shown in FIG. 2, as serialization and deserialization in such a system is implied. Lastly, Figs. 8 and 9 are now entitled: GRANULAR FIFO FILL LEVEL INDICATOR SYSTEM to make these drawing legends consistent with the specification.

Regarding the specification, Applicants have made the suggested modifications. Also, the serial number of the related application has been inserted in the first paragraph of page 1.

Prior to discussing the invention recited in the newly added claims, applicants would like to note fundamental distinctions of their invention over the cited prior art. A

basic plesiochronous data transmission system consists of receiving data and then retransmitting it at almost the same frequency using a local clock. Stuff bits are used to adjust the data rate to match the transmit frequency. This necessitates allocation of "skip" and "stuff" data, which is essentially dummy data that can be inserted or deleted from the data stream to make the data rate match the transmit rate.

The problem with such a prior art system is that the dummy data can over-accumulate or under-accumulate in brief bursts of the data causing the system to fail. For example, even if the transmit frequency matches the received frequency exactly, oscillatory overfill and underfill behavior could occur. This is analogous to how a freeway suddenly loses its ability to flow traffic as the number of cars approaches capacity.

McEachern addresses this problem by using the FIFO fill levels to generate information that allows his system to "smooth out" the usage of stuff bits, so they are evenly distributed over the data stream. This overcomes the problem of localized over-booking. Accordingly, the block diagrams of the MeEachern patent illustrate a mechanism for computation of the optimal instances for insertion of the stuff bits. For example, as illustrated in FIG. 1 (timing and control circuit 16) and FIG. 6 (timing and control circuit 16) of McEachern, stuff control is what is used on systems that do not adjust output frequency and control the data rate through bit stuffing.

As in McEachern, the Nigel patent teaching features bit stuffing and a trivalent phase detector. The trivalent phase detector drives 3 actions (positive justification, do nothing, or negative justification). The do nothing region is optimized to prevent the overstuffing/understuffing oscillatory type behavior.

It is further noted that McEachern features an "analog" phase detector that allows his system to be aware of the relative read phase and write phase with high resolution so that he can compute the optimal location of the stuff bits with high precision.

Regarding this last point, rather than using an "analog" phase detector, Applicants utilize a binary phase detector. However, this is just one aspect of the patentable distinctions over the cited prior art. A fundamental distinction is that rather than bit stuffing, Applicants utilize frequency adjustment. The binary phase detector (e.g. 518 in FIG. 5) sets up the "lock point" for the transmit clock phase locked loop (i.e. the phase detector signals to speed up or slow down the transmit clock). Thus, Applicants' dual loop (PLL/DLL) data synchronization system provides for frequency adjustments of the transmit clock so that stuff data is not necessary. This concept is fundamentally and patentably distinct from the prior art that merely teaches variations of stuff bit techniques. Simply stated, the prior art does not teach bit stream synchronization utilizing a dual loop synchronization system that does not require bit stuffing.

These patentable distinctions are succinctly set forth in the claims as will now be described. Newly added claim 30 recites a dual loop synchronization system (illustrated in e.g. Figs. 5 and 7) as follows:

> 30. (New) A dual loop synchronization system comprising:
>
> a phase lock loop (PLL) having a phase/frequency detector (PFD), a voltage controlled oscillator (VCO), and a phase shifter coupled to said VCO configured in a feedback loop with said PFD, and receiving a local reference clock signal;
>
> a first-in first-out (FIFO) register receiving a parallel data input; and
>
> a delayed lock loop (DLL) having a detector coupled to the output of said FIFO register for detecting the fill level of said FIFO register and a digital loop filter coupled between said detector and said phase shifter of said PLL to produce a phase shift in said PLL. (emphasis added)

As previously noted, the cited prior art does not show the recited combination. As recited in claim 30, applicants provide for a dual loop synchronization system without the use of stuff bits. In particular, the dual loops are used to produce a phase shift in the PLL. This is how applicants adjust the transmit clock and eliminate the need for stuff bits.

In the Office Action, in connection with the rejections under 35USC112 (at paragraph 3), questions were raised in connection with the fill level indicator. (See underlined portion of claim 30: having a detector coupled to the output of said FIFO register for detecting the fill level of said FIFO. By way of clarification, the fill level of FIFO register 522 is detected and indicated by phase detector 518. For example see paragraph [0035] in the specification stating that: "Phase detector 518 in DLL 504 monitors FIFO 522 fill level...". Further, in paragraph [0036]: "Phase detector 518 translates the FIFO fill level into a value that is integrated by loop filter 520 to produce a phase shift in PLL 502". Additional explanation can be found in many other portions of the specification, for example see paragraph [0047] reproduced in its entirety, as follows:

"With continued reference to Figure 7, a detailed discussion of various embodiments suitable for phase detector 718 (as well as phase detector 518 of Figure 5) will follow. As previously mentioned, phase detector 718 is preferably configured to receive an input from FIFO 722 representative of FIFO 722 fill level. In this manner, phase detector 718 may have the function of a 'fill detector' or 'fill level indicator'."

Claim 31 depends from claim 30 and further claims the PLL embedded within the DLL. This is illustrated in FIG. 5. As a further variation, paragraph [0032] states that: "in one particular embodiment, DLL 504 is embedded within PLL 502, however, in other embodiments, the DLL and PLL may be separated."

Claim 32 further describes the detector coupled to the output of said FIFO register for detecting the fill level of said FIFO register as a phase detector (e.g. 518). Claim 33 further describes the detector as a binary phase detector. This not only distinguishes this claim from the McEachern patent but also has the distinctions set forth in paragraph [0038], e.g. "The DLL lends itself well to a fully digital element."

Claim 34 recites that the detector is a wide band phase detector.

Claim 35 recites a loop filter (e.g. 512) coupled between said PFD and said VCO. Claim 36 defines the loop filter as a wide bandwidth loop (as previously recited in canceled claim 28).

Claim 37 recites that the digital loop filter (e.g. 520) is a narrow bandwidth filter (as previously recited in canceled claim 28).

Claim 38 recites details of a counter based dual loop synchronization system having a counter based FIFO fill level indicator as shown, for example, in FIG. 9. Claim 39 recites details of the comparison module claimed in claim 38. Claim 40 recites the embodiment shown in FIG. 11.

As noted hereinabove, claim 30 is believed to recite patentable subject matter. Dependent claims 31-40 are believed to be patentable for the same reasons and also in that they recite additional features not taught by the prior art.

Claims 41-45 succinctly set forth the invention in method terminology and in that sense replace previously presented method claims 13-19 (now canceled). Claim 41 recites as follows:

> . (New) A method for data synchronization in a plesiochronous system comprising the steps of:
>
> receiving write data in a first-in first-out (FIFO) register;
>
> detecting the fill level of the FIFO register at the input of a delay locked loop (DLL);
>
> providing a signal based on the detected fill level to a phase lock loop (PLL);
>
> receiving a local reference clock signal in the PLL;
>
> shifting the phase of the local reference clock signal in the PLL in response to the signal based on the detected fill level provided by the DLL.(emphasis added)

Claim 41 describes the invention in method terminology describing the method steps performed in the FIFO, DLL and PLL to provide data synchronization in a plesiochronous system without bit stuffing. This combination of method steps is not practiced by the prior art and certainly not for the purpose of shifting the phase of the local reference clock signal in the PLL in response to the signal based on the detected fill level provided by the DLL. Claims 42-45 depend from claim 41 and are believed to be allowable for the same reasons and also in that they recite additional features of the invention.

In view of the foregoing, it is believed that claims 30-45 (all the claims currently in this application) are in condition for allowance. If Examiner has a question or comment or if Applicants' attorney can assist in any manner whatsoever, Examiner is respectfully requested to telephone the undersigned

Respectfully submitted,
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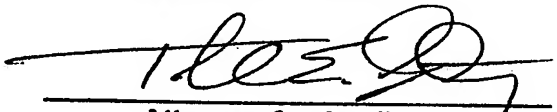

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